REMARKS

The following is intended as a full and complete response to the Final Office Action dated on July 14, 2005. Claims 1-25 were examined. Claims 7-9, 18 and 24 are objected to, but otherwise are indicated to include allowable subject matter.

Claims 1-6, 10-17, 19-23 and 25 are again rejected as anticipated by or obvious over Chu (U.S. Patent No. 5,530,798). Claim 2, 15 and 22 are rejected as unpatentable over Chu further in view of Morein (U.S. Patent No. 6,473,086) or Langendorf (U.S. Patent No. 6,760,031). Finally, claim 25 is rejected under 35 US §103(a) as unpatentable over Chu in view of Rostoker (U.S. Patent No. 5,761,516). All of these rejections are respectfully traversed.

In this Office Action, the Examiner has essentially repeated his analysis and application of the Chu reference. The new explanation of the basis for the response is found at page 6 of the Office Action, where the Examiner replied to the applicant's previous arguments. Therefore, this response will focus on the analysis and argument presented in the Examiner's reply at page 6.

The Examiner, in the first paragraph of page 6, notes that applicant argues that there is no comparison between the dot clock signal 102 in the vertical blanking signal 120 and the synchronizer 60 of the Chu reference. The Examiner now replies that the synchronizer 60 outputs one of the sync signals 18 or 19 and that this is the same as Applicant's teaching in the specification at page 12, line 3-5 that in certain instances, the output sync signal is the external synchronization signal 207, which in the Examiner's view involves no comparison. This re-interpretation of the claims, in the light of the specification is respectfully traversed.

The Examiner cannot contradict the plain language of the claims when that language is clearly supported in the specification. Paragraph [0062] clearly states that the controller 213, is configured to compare the clock signal with an external synchronization signal 207. The same paragraph continues on that the synchronization of the clock signal with the external synchronization signal is described in Fig. 4E and

4F. Turning to those figures, and especially Fig. 4E, paragraph [0086] clearly describes that the controller 213 compares the phase of the clock signal with the phase of the synchronization signal, as claimed. If the phase of the clock signal is not in synchronization with the phase of the synchronization signal 207, then the frequency of the clock generator 215 is adjusted to match the frequency of the synchronization signal 207. In this manner, the timing signal that reaches the GPU is in synchronization with the external synchronization signal 207. Thus, in every case described in Fig. 4E, which is the detailed description supporting the claims at issue, the timing signal provided to the graphics processing unit or module is the result of the comparison between the clock signal with the synchronization signal.

The sentence cited by the Examiner says nothing more than if the phase of the clock signal is in synchronization with the phase of the external synchronization signal 207, then controller 213 transmits the synchronized signal as the timing signal. This does not contradict the fact that a comparison is made in all cases, even though in some cases the comparison will establish that the clock signal and synchronization signal are already in phase and no adjustment is needed. (see, for example, claim 4).

The Examiner concedes in his first paragraph argument on page 6 that in fact there is no comparison taught in the cited Chu reference wherein the choice between signals 18 and 19 being transmitted is simply based on the state of the internal control signal 122. Finally, none of the other references cited by the Examiner provides further support for his rejection.

In view of these clear distinctions, reconsideration and allowance of the claims as presently presented is respectfully requested.

Respectfully submitted,

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